ABSTRACT OF THE DISCLOSURE

Self-aligned split-gate NAND flash memory cell array and process of fabrication in which rows of self-aligned split-gate cells are formed between a bit line diffusion and a common source diffusion in the active area of a substrate. Each cell has control and floating gates which are stacked and self-aligned with each other, and erase and select gates which are split from and self-aligned with the stacked gates, with select gates at both ends of each row which partially overlap the bit line the source diffusions. The channel regions beneath the erase gates are heavily doped to reduce the resistance of the channel between the bit line and source diffusions, and the floating gates are surrounded by the other gates in a manner which provides significantly enhanced high voltage coupling to the floating gates from the other gates. The memory cells are substantially smaller than prior art cells, and the array is biased so that all of the memory cells in it can be erased simultaneously, while programming is bit selectable.